BRIEF DESCRIPTION OF THE DRAWINGS

These and other aspects of the invention will now be described in detail with reference to the accompanying drawings, wherein:

FIG. 1 is a diagram illustrating the architecture of a preferred individual focal plane cell;

FIG. 2 is a plan view of an integrated circuit having a focal plane array of cells of the type illustrated in FIG. 1.

FIG. 3A is a schematic diagram of the cell of FIG. 1.

FIG. 3B is a plan view of an integrated circuit constituting a focal plane array of cells of a type similar to FIG. 1, where the load FET and sampling circuit is deleted from each cell and incorporated as common elements at the bottom of each array column.

FIG. 4 is a graph of the surface potential in the charge transfer section of the cell of FIG. 3A.

FIG. 5 is a cross-sectional view of an alternative embodiment of the focal plane array of FIG. 2 including a micro-lens layer.

FIG. 6A shows a polymer filter embodiment;

FIG. 6B shows a phosphor embodiment;

FIG. 6C is a schematic diagram of an alternate embodiment of the cell of FIG. 3A with a storage well and an

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